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EXAMINER	
GEIB, BENJAMIN P	

ART UNIT	PAPER NUMBER
2181	

NOTIFICATION DATE	DELIVERY MODE
04/15/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTO@wavsip.com

Office Action Summary	Application No.	Applicant(s)	
	10/815,478	BALL, JAMES LORAN	
	Examiner	Art Unit	
	BENJAMIN P. GEIB	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,14,16-19,31 and 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,14,16-19,31 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Applicant, via amendment, has overcome the 35 U.S.C. § 112, second paragraph, rejections set forth in the previous Office Action. Consequently, the examiner has withdrawn these rejections.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Killian et al. (U.S. Patent No. 5,420,992), hereinafter Killian.

4. Regarding claim 1, Killian teaches a processor, comprising:

a plurality of registers *[register file; 42; FIG. 2A]*;

circuitry *[execution unit 15; FIG. 2A]* configured to process a plurality of instructions associated with an instruction set including a plurality of branch and non-branch instructions *[column 7, lines 57-66]*, the plurality of instructions each having a multi-byte length *[all instructions are 32-bit words; column 7, lines 57-66]*, the plurality of instructions accessible at multi-byte aligned addresses *[Because the instructions are 32-bit words (i.e. multi-byte), the instructions are accessed at multi-bye aligned addresses]*;

common subcircuitry *[sign-extension circuit 78; FIG. 3C]* operable to perform sign extensions of an immediate field in non-branch instructions and to perform sign extensions of said immediate fields in branch instructions to calculate a target address for branch instructions, wherein said common subcircuitry operating on said non-branch instructions is the same subcircuitry operating upon said branch instructions *[column 8, lines 7-13, FIG. 3C]*.

wherein the multi-byte aligned branch instructions are operable to access the plurality of instructions at byte aligned addresses *[Because the sign-extended immediate of a branch instruction is added directly to the program counter (column 11, lines 62-64; FIG. 3C), the branch instruction access memory at the same granularity as the program counter, which is the granularity of a byte. Therefore, the branch instructions are operable to access the plurality of instructions at byte aligned addresses]*, wherein each of the multi-byte aligned branch instructions has a start address that is an integer multiple of a byte aligned address and the integer multiple is greater than one *[Because the multi-byte aligned branch instructions are multiple bytes in length, the multi-byte aligned branch instruction have start addresses that are integer multiples of a byte aligned address wherein the integer multiple is greater than one]*.

5. Regarding claim 2, Killian has taught the processor of claim 1, wherein the plurality of instructions are accessed at word aligned addresses *[Because the instructions are 32-bit words (column 5, lines 20-27; column 7, lines 57-66), the instructions are accessed at word aligned addresses]*.

6. Regarding claim 3, Killian has taught a processor of claim 1, wherein the plurality of instructions are accessed at half-word aligned addresses *[Because the instructions are 32-bit words (column 5, lines 20-27; column 7, lines 57-66), the instructions are accessed at half-word aligned addresses]*.

7. Regarding claim 4, Killian has taught the processor of claim 1, wherein accessing the instructions comprises reading to and writing from the addresses *[column 11, lines 62-64]*.

8. Regarding claim 5, Killian has taught the processor of claim 1, wherein the branch instructions comprise branch and conditional branch instructions *[instructions include jump (i.e. branch) and branch (i.e. conditional branch) instructions; column 7, lines 57-66]*.

9. Regarding claim 6, Killian has taught the processor of claim 1, wherein the branch instructions comprise a branch offset and a current program counter value *[column 11, lines 62-64]*.

10. Regarding claim 7, Killian has taught the processor of claim 6, wherein the units of branch offset and a current program counter are in bytes *[column 11, lines 62-64]*.

11. Regarding claim 8, Killian has taught the processor of claim 1, wherein the plurality of instructions are one word in length *[all instructions are 32-bit words; column 5, lines 20-27; column 7, lines 57-66]*.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 14-19, 31, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Killian in view of Wittig et al., "OneChip: An FPGA Processor with Reconfigurable Logic" (hereinafter Wittig).

14. Regarding claim 14, Killian teaches a processor, comprising:

a plurality of registers *[register file; 42; FIG. 2A]*;

circuitry *[execution unit 15; FIG. 2A]* configured to process a plurality of instructions including a plurality of branch instructions and a plurality of non-branch instructions associated with an instruction set *[instructions include jump (i.e. branch), immediate, and register (i.e. non-branch) instructions; column 7, lines 57-66]*, one of the plurality of branch instructions including an immediate field and one of the plurality of non-branch instructions including an immediate field *[column 8, lines 7-13]*;

common subcircuitry *[sign-extension circuit 78; FIG. 3C]* that performs a sign extension of the immediate field associated with the one of the branch instructions and that performs a sign extension of the immediate field associated with the one of the non-branch instructions, wherein said common subcircuitry operating on said non-branch instructions is the same subcircuitry operating upon said branch instructions, wherein the sign extension of the immediate field associated with the one of the branch instructions is performed to determine a branch target address *[column 8, lines 7-13; FIG. 3C]*; wherein each of the plurality of branch instructions and non-branch instructions has a multi-bye length, has a start address that is an integer multiple of a byte aligned address, and is operable to access the plurality of instructions at bye aligned addresses, wherein the integer multiple is greater than one *[Because the sign-extended immediate of a branch instruction is added directly to the program counter (column 11, lines 62-64; FIG. 3C), the branch instruction access memory at the same granularity as the program counter, which is the granularity of a byte. Therefore, the branch instructions are operable to*

access the plurality of instructions at byte aligned addresses. Because the multi-byte aligned branch instructions are multiple bytes in length, the multi-byte aligned branch instruction have start addresses that are integer multiples of a byte aligned address wherein the integer multiple is greater than one].

Killian has not taught that the processor is in a field programmable gate array.

Wittig has taught incorporating a processor within a field programmable gate array *[See Wittig, Introduction].*

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to incorporate the processor of Killian within a field programmable gate array.

The motivation for doing so would be to allow closely coupled access to programmable logic, thereby improving performance of applications requiring the programmable logic *[See Wittig, Introduction].*

15. Regarding claim 16, Killian and Wittig have taught the field programmable gate array of claim 14, wherein the plurality of instructions are accessed at half-word aligned addresses *[Because the instructions are 32-bit words (column 5, lines 20-27; column 7, lines 57-66), the instructions are accessed at half-word aligned addresses].*

16. Regarding claim 17, Killian and Wittig have taught the field programmable gate array of claim 14, wherein branch instructions comprise branch and conditional branch instructions *[instructions include jump (i.e. branch) and branch (i.e. conditional branch) instructions; column 7, lines 57-66].*

17. Regarding claim 18, Killian and Wittig have taught the field programmable gate array of claim 14, wherein the common subcircuitry *[sign-extension circuit 78; FIG. 3C]* is used to handle the immediate field associated with one of the branch instructions and the immediate field associated with the one of the non-branch instructions and wherein an immediate field value of each of the immediate fields is maintained in units of bytes *[Because the sign-extended immediates of branch and non-branch instructions are added directly to the 32-bit program counter and base address, respectively, (column 11, lines 40-64; FIG. 3C), the branch and non-branch immediates are maintained in units of bytes].*

18. Regarding claim 19, Killian and Wittig have taught the field programmable gate array of claim 18, wherein common subcircuitry is used to perform sign-extensions of the immediate field associated with the branch and non-branch instructions *[sign-extension circuit 78; FIG. 3C; column 11, lines 40-64]*.

19. Referring to claim 31, Killian has taught the processor of claim 1, wherein one of a primary or secondary component accesses memory of the processor directly through ports without access through a system bus *[FIG. 1]*.

Killian has not taught that the processor is implemented on a field programmable gate array that does not comprise a system bus.

Wittig has taught incorporating a processor within a field programmable gate array that does not comprise a system bus *[See Wittig, Introduction]*.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to incorporate the processor of Killian within a field programmable gate array as taught by Wittig.

The motivation for doing so would be to allow closely coupled access to programmable logic, thereby improving performance of applications requiring the programmable logic *[See Wittig, Introduction]*.

20. Referring to claim 32, Killian and Wittig have taught the field programmable gate array of claim 14, wherein one of a primary or secondary component accesses memory of the field programmable gate array directly through ports without access through a system bus, and wherein the array does not comprise a system bus *[FIG. 1]*.

Response to Arguments

21. Applicant's arguments filed 01/04/2010 have been fully considered but they are not persuasive.

22. Applicant argues the novelty/rejection of the claims, in substance, that "Killian does not disclose or suggest a multi-byte aligned branch instruction having a start address that is an integer multiple, greater than one, of a byte aligned address and this branch instruction is operable to access an instruction at a byte aligned address." The Examiner disagrees. Killian has taught 32-bit (i.e. multi-byte) branch instructions. See column 7, lines 57-66. These multi-byte branch instructions access target

instructions using an immediate value that is signed-extended and then added directly to the 32-bit program counter. See column 11, lines 62-64; FIG. 3C. Because the sign-extended immediate of a branch instruction is added directly to the program counter, the branch instructions access memory at the same granularity as the program counter, which is the granularity of a byte. Therefore, the branch instructions are operable to access the plurality of instructions at byte aligned addresses. Further, because the multi-byte aligned branch instructions are multiple bytes in length, the multi-byte aligned branch instruction have start addresses that are integer multiples of a byte aligned address wherein the integer multiple is greater than one.

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BENJAMIN P. GEIB whose telephone number is (571)272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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